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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/724,865	11/28/2000	Stephen M. Trimberger	X-805-2 US	8383

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EXAMINER	
SMITHERS, MATTHEW	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,865	TRIMBERGER ET AL.	
	Examiner	Art Unit	
	Matthew B Smithers	2137	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

The information disclosure statement filed October 18, 2004 has been placed in the application file and the information referred to therein has been considered as to the merits.

Claim Rejections - 35 USC § 102

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. patent 5,970,142 granted to Erickson and further in view of U.S. patent 5,764,076 granted to Lee et al.

Regarding claims 1-4, Erickson teaches a programmable logic device that includes a decryption circuit (decryptor) for decrypting encrypted configuration bitstream using a decryption key loaded without a loading design or the assistance of a device programmer (see column 7, line 36 to column 8, line 32). However, Erickson fails to specifically teach testing the printed circuit board attached to programmable logic device

prior to loading of the decryption key. Lee teaches configuring a programmable logic device (PLD) that is "in-system" (installed on a printed circuit board), while verifying the integrity (testing) of the printed circuit board through the use of the JTAG port (see column 1, lines 41-51; column 2, lines 36-46 and column 2, line 66 to column 3, line 12. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lee's method of reprogramming configuration data to a PLD with Erickson's method of communicating configuration data to a PLD in order to avoid disconnecting or suspending authorized programmable logic devices from normal operations while loading or reprogramming the devices with a new decryption key [see Lee et al.; column 1, lines 41-52].

Regarding claim 5, Erickson as modified teaches the PLD has the test access port is a JTAG port (see Lee; column 2, lines 36-46; Figure 1, element 115 and Figure 2).

Regarding claim 6, Erickson as modified teaches configuring the PLD for a non-secure mode prior to the loading the decryption keys; and configuring the PLD for a secure mode after the loading the decryption keys (see Lee; column 2, lines 36-60).

Regarding claim 7, Erickson as modified teaches erasing the decryption keys from the memory when configuring the PLD for the non-secure mode (see Lee; column 2, lines 36-60).

Regarding claim 8, Erickson as modified teaches clearing a design from a configuration memory of the PLD when configuring the PLD for the non-secure mode (see Lee; column 2, lines 36-60).

Regarding claim 9, Erickson as modified teaches reading the decryption keys using the JTAG port for verification (see Lee; column 2, lines 36-60).

Regarding claim 10, Erickson as modified teaches a decryptor for decrypting an encrypted bitstream using the at least one decryption key (see Erickson; column 7, line 36 to column 8, line 32).

Regarding claim 11, Erickson as modified teaches a key memory for storing the at least one decryption key (see Erickson; column 7, line 36 to column 8, line 32).

Regarding claim 12, Erickson as modified teaches programmable logic; configuration memory coupled to the programmable logic for configuring the programmable logic to perform a desired function; and configuration logic coupled between the decryptor and the configuration memory for providing programming information to the configuration memory; wherein the programming information comprises at least a portion of a decrypted bitstream provided by the decryptor (see Erickson; column 7, line 36 to column 8, line 32).

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. patent 6,118,869 granted to Kelem et al. and further in view of U.S. patent 5,764,076 granted to Lee et al.

Regarding claims 1-4, Kelem teaches a programmable logic device (FPGA) that includes a means for decrypting (decryptor) encrypted configuration bitstream after loading of the decryption key without a loading design or the assistance of a device programmer (see column 1, lines 10-16; column 1, lines 55-61; and column 3, ines 14-

43). However, Kelem fails to specifically teach testing the printed circuit board attached to programmable logic device prior to loading of the decryption key. Lee teaches configuring a programmable logic device (PLD) that is "in-system" (installed on a printed circuit board), while verifying the integrity (testing) of the printed circuit board through the use of the JTAG port (see column 1, lines 41-51; column 2, lines 36-46 and column 2, line 66 to column 3, line 12. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lee's method of reprogramming configuration data to a PLD with Kelem's method for PLD bitstream decryption in order to avoid disconnecting or suspending authorized programmable logic devices from normal operations while loading or reprogramming the devices with a new decryption key [see Lee et al.; column 1, lines 41-52].

Regarding claim 5, Kelem as modified teaches the PLD has the test access port is a JTAG port (see Lee; column 2, lines 36-46; Figure 1, element 115 and Figure 2).

Regarding claim 6, Kelem as modified teaches configuring the PLD for a non-secure mode prior to the loading the decryption keys; and configuring the PLD for a secure mode after the loading the decryption keys (see Lee; column 2, lines 36-60).

Regarding claim 7, Kelem as modified teaches erasing the decryption keys from the memory when configuring the PLD for the non-secure mode (see Lee; column 2, lines 36-60).

Regarding claim 8, Kelem as modified teaches clearing a design from a configuration memory of the PLD when configuring the PLD for the non-secure mode (see Lee; column 2, lines 36-60).

Regarding claim 9, Kelem as modified teaches reading the decryption keys using the JTAG port for verification (see Lee; column 2, lines 36-60).

Regarding claim 10, Kelem as modified teaches a decryptor for decrypting an encrypted bitstream using the at least one decryption key (see Kelem; column 3, lines 14-47).

Regarding claim 11, Kelem as modified teaches a key memory for storing the at least one decryption key (see Kelem; column 3, lines 14-47).

Regarding claim 12, Kelem as modified teaches programmable logic; configuration memory coupled to the programmable logic for configuring the programmable logic to perform a desired function; and configuration logic coupled between the decryptor and the configuration memory for providing programming information to the configuration memory; wherein the programming information comprises at least a portion of a decrypted bitstream provided by the decryptor (see Kelem; column 3, lines 14-47).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew B Smithers whose telephone number is (571) 272-3876. The examiner can normally be reached on Monday-Friday (8:00-4:30) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew T Caldwell can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew B Smithers
Primary Examiner
Art Unit 2137